

We claim:

- 1 1. A decoder comprising:
2 a SISO device that operates as a PCCC decoder in a first mode of operation and
3 as an SCCC decoder in a second mode of operation where the device operates as per at
4 least one trellis using an in-line addressing technique to process information.
- 1 2. The processor of claim 1 where the device processes information in accordance with
2 an algorithm.
- 1 3. The processor of claim 2 where the algorithm is a Log MAP algorithm and the SISO
2 device is a Log MAP processor.
- 1 4. The processor of claim 1 where in the first mode of operation the SISO device
2 operates as a first SISO during one time period and operates as a second SISO device
3 where the first and second SISO devices process information as per the same or different
4 trellis.
- 1 5. The processor of claim 1 where in the second mode of operation the SISO device
2 operates as an inner SISO during one time period whereby it processes information as per
3 a first trellis and operates as an outer SISO during another time period whereby it
4 processes information as per a second trellis.
- 1 6. The processor of claim 5 where the first trellis is a N_1 -state Radix-K trellis and the
2 second trellis is a N_2 -state Radix-K trellis where N_1 may or may not equal to N_2 and K,
3 N_1 and N_2 are integers equal to 1 or greater.

- 1 7. The processor of claim 1 where the SISO processor comprises:
 - 2 at least one branch metric calculator;
 - 3 at least one forward path metric calculator and least one backward path metric
 - 4 calculator where both calculators are in communication with the branch metric calculator;
 - 5 at least one Log Likelihood calculator coupled to the path metric calculators; and
 - 6 at least one subtractor circuit having an extrinsic information input and coupled to
 - 7 the at least one Log Likelihood calculator to provide at least one Log Likelihood ratio
 - 8 output whereby the path metric calculators and the at least one Log Likelihood calculator
 - 9 are constructed with Log Sum operators which are designed based on an approximation
 - 10 of a Jacobian definition of a Log Sum operation.
- 1 8. The processor of claim 7 in which the information is processed as per an N_1 state
- 2 Radix-K first trellis and an N_2 state Radix-K second trellis when operating as an SCCC
- 3 turbo decoder where N_1 is not equal to N_2 and where N_1 and N_2 are integers equal to 2 or
- 4 greater and K is an integer equal to 4 or greater.
- 1 9. The processor of claim 7 where the SISO processor is operating as a PCCC decoder
- 2 and N_1 may not be equal to N_2 and K is an integer equal to 4 or greater and N_1 , N_2 are
- 3 integers equal to 2 or greater.
- 1 10. The processor of claim 1 where the in-line addressing technique uses a block of
- 2 memory for retrieving and storing values of the states of the trellis as the device
- 3 processes the received information.
- 1 11. The processor of claim 1 where information is processed using a portion of the states
- 2 of the trellis to perform the in-line addressing technique during a clock cycle.
- 1 12. A method of performing turbo decoding, the method comprising the step of:
- 2 processing, in accordance with an algorithm, received information as per an N-
- 3 state Radix-K trellis using an in-line addressing technique where N, K are integer equal
- 4 to 1 or greater.

- 1 13. The method of claim 12 where the received information is processed as per an N-
2 state Radix-K trellis using an in-line addressing technique where N is an integer equal to
3 2 or greater and K is an integer equal to 4 or greater.

- 1 14. The method of claim 12 where the in-line addressing technique uses a block of
2 memory to retrieve and store states of the trellis as information is processed per the
3 trellis.